REMARKS

Prior to examination on the merits, please amend the specification as indicated above. Claims 21-29 are pending in the present application.

CONCLUSION

In view of the foregoing, it is respectfully submitted that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number, in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

Please charge any shortage in fees due in connection with the filing of this communication to Deposit Account No. 50-0206, and please credit any excess fees to such deposit account.

Respectfully submitted,

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APPENDIX A

1-20 (Cancelled).

21 (New). A circuit comprising:

an output driver;

a data receiver;

a clock receiver for receiving a clock signal; and

a calibration path selectively configurable to couple one of the data receiver and the clock receiver to the output driver based at least in part upon the clock signal.

22 (new). The circuit of claim 21, wherein the clock signal comprises an embedded command, wherein the calibration path is selectively configurable to couple one of the data receiver and the clock receiver to the output driver based at least in part upon the embedded command.

23 (new). The circuit of claim 22, further comprising:

a first multiplexer coupled to the data receiver and the clock receiver, the first multiplexer passing the clock signal received by the clock receiver when a first multiplexer control signal is in a first logic state, and passing an input data

signal received by the data receiver when the first multiplexer control signal is in a second logic state.

24 (new). The circuit of claim 23, further comprising:

a second multiplexer coupled to the first multiplexer and the output driver, the second multiplexer passing a signal output from the first multiplexer when a second multiplexer control signal is in a first logic state, and passing an output data signal when the second multiplexer control signal is in a second logic state, the signal output from the first multiplexer being the clock signal when the first multiplexer control signal is in the first logic state, and being the input data signal when the first multiplexer control signal is in the second logic state.

25 (new). The circuit of claim 24, further comprising:

a serial-to-parallel shift register coupled to the data receiver, the clock signal clocking the serial-to-parallel shift register.

26 (new). The circuit of claim 25, further comprising:

a parallel-to-serial shift register coupled to the second multiplexer, the parallel-to-serial shift register providing the

output data signal to the second multiplexer, the clock signal clocking the parallel-to-serial shift register.

27 (new). The circuit of claim 26, further comprising:

a logic circuit coupled to the first multiplexer, the second multiplexer, and the parallel-to-serial shift register, the logic circuit receiving the clock signal and setting the logic states of the first and second multiplexer signals based at least in part upon the embedded command.

28 (new). The circuit of claim 26, further comprising:

a logic circuit coupled to the first multiplexer, the second multiplexer, and the parallel-to-serial shift register, the logic circuit receiving the clock signal and outputs a data pattern to the parallel-to-serial shift register based at least in part upon the embedded command.

29 (new). The circuit of claim 26, further comprising:

an internal circuit coupled to the clock receiver, the serial-to-parallel shift register, and the parallel-to-serial shift register, the internal circuit receiving the clock signal received by the clock receiver, receiving parallel input data

from the serial-to-parallel shift register, and outputting parallel output data to the parallel-to-serial shift register.